IN THE CLAIMS

Claims 1-49 (cancelled)

50. (New) A processing device comprising:

a reconfigurable circuit including a plurality of data processing units,

an internal state holding circuit for holding data being processed inside each of the data processing units,

a memory portion for storing data provided from outputs of the data processing units, and

a data processing unit of the plurality of the units includes multiple data processing sub-units, wherein:

data from an output of a first data processing sub-unit of the multiple data processing sub-units is supplied to the internal state holding circuit before being supplied to an input of a second data processing sub-unit of the multiple data processing sub-units, and

data from an output of a first data processing unit of the plurality of the data processing units is supplied to the memory portion before being supplied to an input of a second data processing unit of the plurality of the units.

51. (New) The device of claim 50, wherein

the first data processing sub-unit is allocated to perform a first operation and the second data processing sub-unit is allocated to perform a second operation, and

when the second data processing sub-unit is not involved in performing the second operation, the second data processing sub-unit is reallocated to perform a third operation.